REMARKS

Applicants have amended Claims 18, 19, 21, 22, and 24 and, therefore, upon entry of this response, Claims 1-35 are pending. Applicants respectfully request reconsideration and reexamination of the application.

Claims 1-35 were rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,851,047 to Fox et al. [herein referred to as "Fox"]. Applicants believe that Fox should be cited under 102(e) rather than 102(a) as Fox was not published prior to the filing date of the present application.

Examiner indicates that Fox teaches "non-volatile memory (203) adapted to store data which is transferable to the volatile memory to configure the programmable logic device" (OA pg. 2). Applicants respectfully disagree as Fox discloses that external memory device 103 (Fig. 1) stores the logic values for the configuration memory cells (col. 4 lns. 25-30) or RAM 202 (col. 6 lns. 60-65). Furthermore, Fox clearly sets forth that "[i]f memory device 103 is disconnected, then CSoC 101 must have been previously programmed, i.e. all values already loaded into the configuration memory cells, and a reset function triggered" (col. 5 lns. 5-12). Thus, Fox does not teach or disclose storing configuration data in the non-volatile memory for transfer into the configuration memory cells (volatile memory) of CSL 201.

Consequently, Fox fails to teach or disclose "non-volatile memory adapted to store data which is transferable to the volatile memory to configure the programmable logic device" as recited in Claim 1, "flash memory adapted to store data which is transferable to the static random access memory to configure the programmable device" as recited in Claim 12, "providing a direct mode for transferring the external configuration data via the second data port to the non-volatile memory" as recited in amended Claim 18, "non-volatile memory

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adapted to store data which is transferable to the volatile memory to configure the programmable logic device" as recited in Claim 25, and "providing data registers adapted to transfer data stored in the non-volatile memory to the volatile memory and to transfer data stored in the volatile memory to the non-volatile memory" as recited in Claim 31.

Therefore, Applicants respectfully submit that Claims 1, 12, 18, 25, and 31 patentably distinguish over Fox and that corresponding dependent claims are also distinguishable for at least the same reasons. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 102(a) of Claims 1-35 be withdrawn.

Claims 1-35 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,828,823 to Tsui et al. [herein referred to as "Tsui"].

Examiner indicates that Tsui teaches "a second data port (JTAG connected to 210 of figure 2) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory" (OA pg. 7). Applicants respectfully disagree as Fig. 2 of Tsui simply illustrates figuratively that JTAG data path 206 may be used to program EE cells 202, while static RAM cells 204 may be programmed via a data path 210 directly via a JTAG port and/or a data port (e.g., a CPU port) (col. 3, lns. 54-65). This is more clearly illustrated in Fig. 3 of Tsui, which shows data port 302 (e.g., JTAG port) useable to program EEPROM 306 or SRAM 308, but data port 304 (e.g., CPU port) useable to program only SRAM 308.

Consequently, Tsui fails to teach or disclose "a second data port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory" as recited in Claim 1, "a CPU port adapted to receive external data for transfer into either the static random access memory or the flash memory" as recited in Claim 12, "providing a direct mode for transferring the external data via the second data port to the non-volatile memory"

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as recited in Claim 18, "a CPU port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory" as recited in Claim 25, and "providing a CPU port adapted to receive external data for transfer into either volatile memory or non-volatile memory of the programmable logic device" as recited in Claim 31.

Therefore, Applicants respectfully submit that Claims 1, 12, 18, 25, and 31 patentably distinguish over Tsui and that corresponding dependent claims are also distinguishable for at least the same reasons. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 102(e) of Claims 1-35 be withdrawn.

Accordingly, Applicants respectfully submit that Claims 1-35 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

Certificate of Mailing

I hereby certify that this correspondence is being mailed via First Class Mail to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, Mail Stop Amendment, on the date stated below.

Tina Kavanaugh

November 23, 2005

Respectfully submitted,

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IN THE DRAWINGS

Applicants submitted formal drawings with the patent application. With this response, Applicants are submitting a replacement sheet to correct a typographical error "Contol" for Control Logic 106 in Fig. 1. No new matter is being added and support may be found in the informal figures and in the corresponding text for Fig. 1. Applicants respectfully request Examiner's review and acceptance of the formal drawings previously submitted and this replacement sheet for the formal drawings.

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